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International Journal of Thermal Sciences 42 (2003) 533–539

International Journal of Thermal Sciences

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Developing an equivalent thermal model for discrete semiconductor packages

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Received 5 March 2001; accepted 11 January 2002

Abstract

The paper covers a useful and practical method for users of power semiconductor devices to derive dynamic thermal models of discrete semiconductor packages. Derivation is based on transient thermal impedance responses measured experimentally or deduced from semiconductor manufacturer data-sheets. Such dynamic thermal models are required for electro-thermal simulation of power electronic circuits corresponding to short power pulse excitations. Indeed in such excitations, the main transient phenomena occur inside the semiconductor die. Contrarily to classical thermal models based on simple resistor/capacitor cells, the proposed model is a behavioral thermal model based on the finite element modeling of the semiconductor chip. It takes into account the main thermal temperature-related non-linearities of package layers. The derived thermal models offer an excellent trade-off between accuracy, efficiency and CPU-cost.
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Keywords: Thermal model; Discrete semiconductor packages; Thermal impedance; Power surges

1. Introduction

Deriving dynamic models from thermal impedance data of packaged semiconductor devices is useful to evaluate the junction temperature of these devices during operation. Such models should take into account the package thermal impedance including the silicon chip, the die attach layers and the heat spreader.

Junction-to-case thermal impedance can be measured experimentally and they are available on semiconductor manufacturer data sheets. These data are used from several tens of years to estimate (by hand) the junction temperature knowing the average power losses. In Power Electronic applications, power losses may be represented by cyclic step functions. The transient thermal impedance curves give the increase in junction temperature as a function of the peak value, the duration and the duty cycle of power loss input waveforms.

However such transient thermal impedance curves do not fit with time-domain simulation, like those involved in circuit simulators.

So time-domain thermal models are required to achieve electro-thermal simulations of power systems. They are compatible with circuit simulators in which most of the semiconductor device models are implemented. The present paper objectives are two-fold.

- Building an equivalent thermal model of a discrete device using the step transient thermal impedance curves.
- Taking into account the non-linearities of the thermal conductivity of the silicon die. This allows a better estimation of the peak junction temperature.

The proposed thermal model has a strong physical meaning and gives accurate thermal responses even in the practical case where the dissipated power duration is in the range of few microseconds to some hundreds of millisecond. The model is equivalent to a discretization of the 1-D heat equation by the finite element method. It is represented by a cir-

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doi:10.1016/S1290-0729(02)00053-4

Nomenclature

c	material specific heat	$J\cdot kg^{-1}\cdot K^{-1}$
h	discretisation step	m
k	thermal conductivity	$W\cdot m^{-1}\cdot K^{-1}$
k_{Si0}	the thermal conductivity of silicon at $T = 300$ K	$W\cdot m^{-1}\cdot K^{-1}$
L	effective thickness of the material	m
P	dissipated power	W
P_0	magnitude of the dissipated power $P(t)$	W
R	duty cycle of the dissipated power signal	
R_{th}	thermal resistance	$K\cdot W^{-1}$
R_{thJ-A}	thermal resistance between junction and air	$K\cdot W^{-1}$
S	effective area of the material	m^2
T	absolute temperature	K
T_j	junction temperature	K
T_c	case temperature	K
T_A	ambient temperature	K
$T_{(\infty,\infty)}$	temperature at $x = \infty$ and time $= \infty$	K
T_{in}	input temperature	K
Z_{th}	transient thermal impedance	$K\cdot W^{-1}$
Z_{thJ-C}	transient thermal impedance between junction and case	$K\cdot W^{-1}$
Z_{thJ-A}	transient thermal impedance between junction and air	$K\cdot W^{-1}$
ρ	material mass density	$kg\cdot m^{-3}$
τ	dissipated power pulse duration	s
α	thermal diffusivity	$m^2\cdot s^{-1}$

cuit networks which fit well with commercially available circuit simulators.

The first section presents the transient thermal impedance: a common concept of electronic device package. Section 2 presents a modeling-oriented analysis of the package of some IGBT devices (TO220 package). The identification of the effective geometric characteristics of the different layers is presented in Section 3.

Section 4 covers the device temperature responses at different depths inside the package. The effect of non-linearities of the silicon thermal conductivity on temperature responses is studied. The final section concerns the device behavior in the case of large power surges of short time duration. Discussion about the thermal model accuracy is presented.

2. Equivalent thermal model of a discrete power device package

2.1. Transient thermal impedance

Transient thermal impedance is a concept used for many years in semiconductor manufacturer datasheets [1]. Details for the concept of transient thermal impedance may be found in [2]. The generated heat flow, $P(t)$, at the top surface, $x = 0$, through a semi-infinite solid is described by the classical temperature expression $T(x,t)$ given by (1)

$$T(x=0,t) = T_{(\infty,\infty)} + \frac{1}{\rho c\sqrt{\pi\alpha}}\int_0^t P(t-\varphi)\frac{d\varphi}{\sqrt{\varphi}} \qquad (1)$$

Moreover, in the particular but practical case of power losses with rectangular waveforms featuring an amplitude P_0, the top surface temperature is given by (2)

$$T(x=0,t) = T_{(\infty,\infty)} + \frac{2P_0}{\rho c\sqrt{\pi\alpha}}\sqrt{t} \qquad (2)$$

finally,

$$T_{(0,\infty)} = T_{(\infty,\infty)} = Z_{th}\cdot P_0 \qquad (3)$$

where Z_{th} is the transient thermal impedance of the semi-infinite solid.

In the case of periodic pulsed power losses, the transient thermal impedance depends on the waveform duty ratio. Indeed experimental measurements show the validity of (3) even in the case of complex packages as shown in Fig. 1. So for many years, (3) is used to characterize the junction-to-case transient thermal behavior when designing thermal paths of Power Electronic applications. However, such an approach is not compatible with circuit simulators demanding differential and algebraic equations to represent device transient models.

The present paper focuses on the use of available data on the transient thermal impedance to build behavioral thermal models of semiconductor devices for Power Electronic system simulation and design.

The definition of the junction-to-ambient thermal impedance Z_{thJ-A} characterizing a thermal system is given by (4)

$$Z_{thJ-A}(\tau, R) = (T_j - T_A)/P \qquad (4)$$

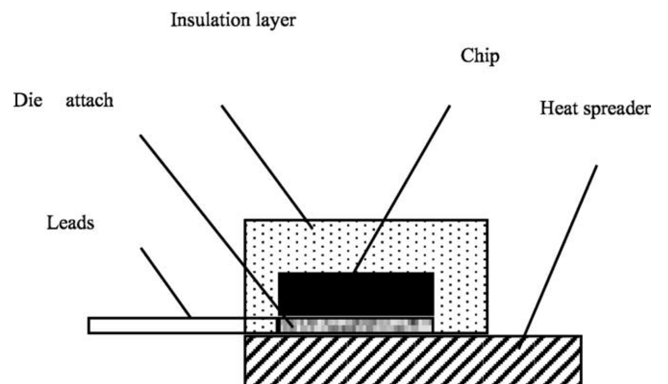

Fig. 1. The studied discrete devices package.

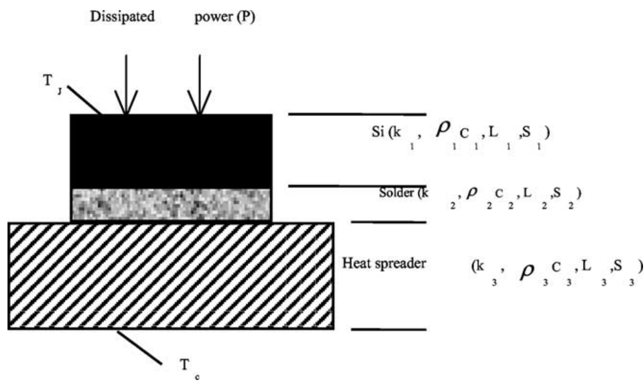

Fig. 2. Geometrical and thermal structure description of the studied devices.

where T_{j} is the hot spot temperature, T_{A} is the ambient temperature. P, τ and R are respectively the peak value, the duration and the duty cycle of the top surface heat generation $P(t)$.

For large value of the duration, τ, $Z_{\mathrm{thJ-A}}$ reaches the junction-to-ambient thermal resistance, $R_{\mathrm{thJ-A}}$. The thermal impedance curves are classically given for different duty cycle values and in the range of few microseconds to some hundreds of millisecond for the pulse duration.

Sometimes, semiconductor manufacturers give only the step transient thermal response ($R = 1$) of the devices. These data do not include values for τ lower than few microseconds.

2.2. Modeling the thermal system

A thermal model, compatible with circuit simulators is required to represent data available from transient thermal impedance.

Most discrete power semiconductor devices (without electrical insulator between chip and case) comprise three main components: a silicon die, a die attach and a spreader. Fig. 1 shows the different components constituting the IGBT IRGBC 20U (13 A/600 V).

When the power pulse durations are small, the evolution of the thermal impedance curves is very sensitive to duty cycle variations. In these conditions the temperature gradient inside the device is large especially in the silicon die.

Moreover, in the case of a vertical power device, the electrical power is dissipated at the top of the silicon die (device active region). Heat flows from the top surface (S_1) mainly in a perpendicular direction (Fig. 2). So, a one-dimensional heat flow may be considered [2] for the silicon layer (Fig. 3).

In normal operating conditions, the silicon layer temperature is not too high ($<150\,^{\circ}\mathrm{C}$), so it is assumed that the thermal characteristics of the device are independent of temperature. Since the other layers inside the package have a higher thermal conductivity, thermal radiation and convection occurring at the package top surface area second order phenomena. However it may be classically represented by a junction-to-ambient equivalent thermal resistor [3,4]. Radiation and convection phenomena are not considered here.

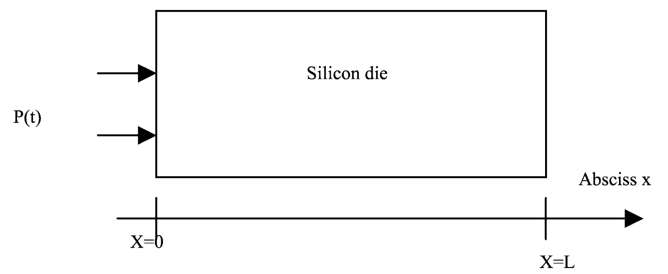

Fig. 3. Unidimensional semiconductor die representation considered for the thermal modeling.

Die attach and heat spreader modeling is considered. Heat flow is not one-dimensional, but in practice these layers act only on the long-term behavior of the package (several milliseconds). Our purpose is not to design heat spreaders but to model the electro-thermal couplings inside the power semiconductor devices. So accurate maps of the temperature inside the die attach and the heat spreader are not useful. Only a junction-to-case behavior is needed. Thus it has been chosen to represent each layer using the one-dimensional heat flow equation. We propose an accurate representation of the one-dimensional heat flow inside the silicon layer and a behavioral one-dimensional heat flow model for the other layers. It will be shown that a good overall behavioral thermal model of the package is obtained, fully compatible with power converter design requirements.

Finite element modeling of heat flow through a 1D-layer

One-dimensional heat flow phenomena in a solid layer are governed by the following partial differential equation (5).

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}(t,x)\right) = \rho c\frac{\partial T}{\partial t}(t,x) \tag{5}$$

With the boundary conditions

$$Sk\frac{\partial T}{\partial x}\bigg|_{x=0} = -P(t) \tag{6a}$$

$$T(t, x = L) = T_{\mathrm{in}}(t) \tag{6b}$$

where $T_{\mathrm{in}}(t)$ is the input temperature and $P(t)$ is the input dissipated power.

In [5,6] the authors show that the thermal model circuit network equivalent to the discretization of the 1-D heat equation by the finite element method is a good candidate for junction temperature estimation.

The state-space approximated solution of (5) is given by

$$\widetilde{T}(x,t) = \sum_{i=1}^{m} \xi_i(t) W_i(x) \tag{7}$$

where $W_i(x)$ are decomposition functions and $\xi_i(t)$ are the coordinates of the temperature approximation in the functional-space basis formed by the decomposition functions.

A trial function $S_i(x)$ is considered. Using (5), (6) and (7) to integrate (4) multiplied by a trial function $S_i(x)$ over $[0, L]$ yield the matrix form (8)

$$M\dot{\xi} + R\xi = Bu \tag{8}$$

where

$$M_{ij} = \int_0^L W_j(x) S_i(x)\,\mathrm{d}x$$

$$R_{ij} = \frac{k}{\rho c}\int_0^L \frac{\mathrm{d}W_j}{\mathrm{d}x}\frac{\mathrm{d}S_i}{\mathrm{d}x}\,\mathrm{d}x - \frac{k}{\rho c}\frac{\mathrm{d}W_j(L)}{\mathrm{d}x}S_i(L)$$

$$B_i = \frac{S_i(0)}{\rho c S}$$

Particularly the Finite Element Method (FEM) consists in a trivial choice of the decomposition functions $W_i(x)$, as linear piecewise functions, equal to 1 at node number i, and zero at any other node (Fig. 4). In our case, $\xi_i(t)$ corresponds to the temperature value at node, i. Classically the trial functions, $S_i(x)$, are chosen to be equal to the decomposition functions $W_i(x)$.

For the chosen $W_i(x)$ functions and between nodes i and $i+1$, (8) gives

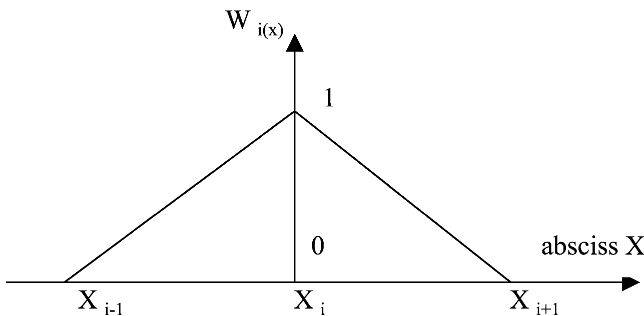

Fig. 4. Distribution function $W_i(x)$ used in the FEM.

$$\rho c h S\begin{pmatrix} 1/3 & 1/6 \\ 1/6 & 1/3 \end{pmatrix}\begin{pmatrix} \dot{\xi}_i \\ \dot{\xi}_{i+1} \end{pmatrix} + kS/h\begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix}\begin{pmatrix} \xi_i \\ \xi_{i+1} \end{pmatrix} = 0 \tag{9}$$

Fig. 5 pictures the circuit network equivalent to the proposed equivalent thermal circuit used to estimate the thermal behavior of the studied device (including package). For more details refer to [5,6].

For the silicon layer (characterized by k_1, ρ_1 c_1, S_1 and L_1), for example, the network components are

$$R_{1\mathrm{Si}} = \frac{L_1}{(n-1)k_1 S_1}, \qquad C_{1\mathrm{Si}} = \frac{\rho_1 c_1 S_1 L_1}{2(n-1)}$$

$$C_{2\mathrm{Si}} = -\frac{\rho_1 c_1 S_1 L_1}{6(n-1)}$$

where (n) is the number of nodes in the silicon die model.

2.3. Identification of the model parameters

The effective dimensions of the different package components are obtained by applying an identification method to obtain the optimal parameter set (p) for the proposed model. The procedure is based on the minimization of a quadratic error criterion J. The latter value is obtained by comparing the experimental junction temperature response T_j and the simulation results given by the system model, $\widetilde{T}_j(p)$, for the parameter set (p). The parameters to be identified are the effective thickness and area (L, S) of each layer inside the package. The temperature response T_j is obtained by means of experimental set-up or by computing its value from the step transient impedance curve, Z_{th}, given by the manufacturer datasheets as follows,

$$T_j = T_c + Z_{th}P \tag{10}$$

where $P(t)$ is the dissipated power at the device top surface. The criterion J is given by

$$J(p) = \left[\frac{1}{t_2 - t_1}\int_{t_1}^{t_2}\left(\widetilde{T}_j(p) - T_j\right)^2 \mathrm{d}t\right]^{1/2} \tag{11}$$

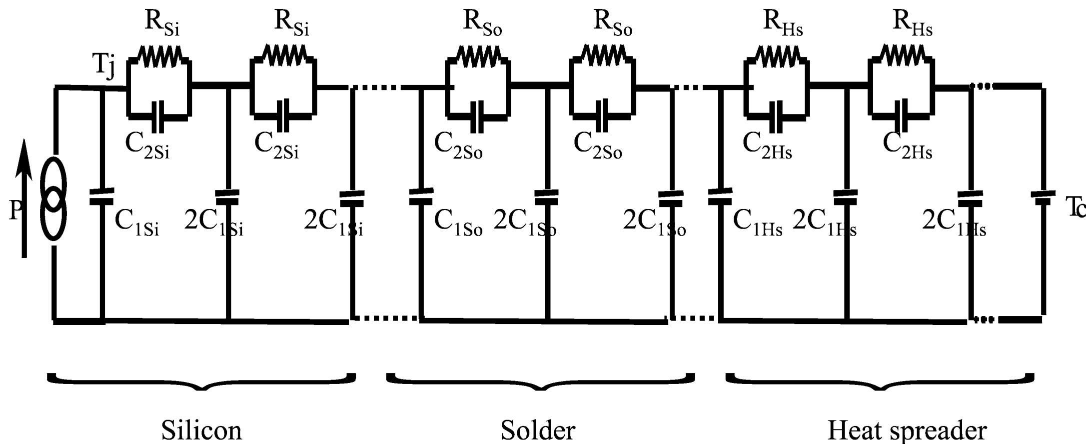

Fig. 5. The proposed FEM thermal model of the discrete device package for thermal characterization.

where t_1 and t_2 are the time boundaries of the thermal response curve $T_j(t)$. The relaxation algorithm with inequality constraints [7,8] has been applied for model parameter identification (geometrical dimensions). Table 1 lists the thermal characteristics of the different components constituting the studied devices and the identified parameters.

Fig. 6 shows the step thermal impedance curves obtained by simulation and from the manufacturer data-sheets (for the IGBT IRGBC20U) for the case $R = 1$. The thermal impedance evolution, for a power cycling condition (duty cycle $R = 0.5$) is obtained by the presented thermal model.

Using the proposed model, any thermal impedance can be estimated for various duty cycle values, and especially those not given by the semiconductor manufacturer data-sheets.

Next section presents the effect of the thermal conductivity non-linearities on the accuracy of the estimated peak temperature evolution inside the device silicon die.

2.4. Discussion

The proposed technique has been applied to three devices which have different current/voltage ratings (Table 1). The technique may be applied equally to any vertical structure in discrete package as MOSFET and IGBT transistors which are preferably used in Power Electronic applications.

The proposed model is behavioral, but a good representation of the silicon part is required to obtain accurate results. A 12-order FEM model is used for the silicon chip.

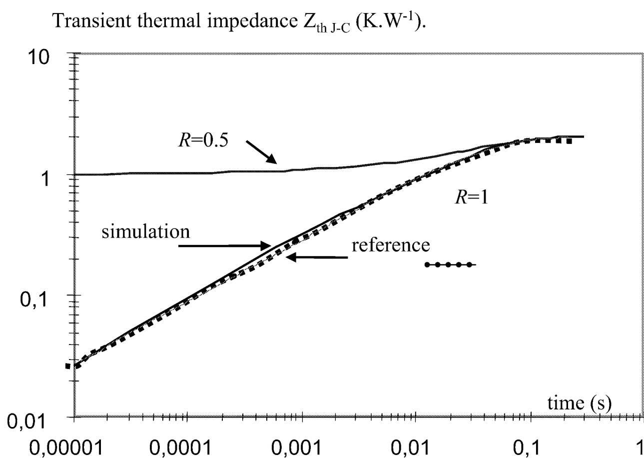

Fig. 6. Comparison between the Z_{thJ-C} reference curve with the simulated one obtained after the parametric identification procedure (IRGBC 20U).

The model order for the chip bounding parts, and the heat spreader are respectively 2 and 4. The chosen model-orders are sufficient to predict the peak junction temperature inside the device under large power surge conditions. The use of a thermal model order greater than 12 for silicon does not participate significantly to the improvement of the thermal response accuracy.

3. Thermal response of the device at different depths inside the package

The power step or cycling thermal impedance curves given by semiconductor manufacturer data-sheets are independent of the power losses. This implies that the thermal conductivity of the different package layers are independent of the temperature.

This section covers the study of the effects of the thermal parameter temperature-dependencies on the accuracy of the peak junction temperature estimation.

Fig. 7 shows the studied device attached to an external heat sink. The studied devices are supposed to be fixed to the heat sink via the case. To simplify the representation of the case to air thermal model, the convection coefficient is supposed to have a large value. The equivalent thermal resistance of the contact to the heat sink, and the heat sink is assumed to be equal to 1 °C·W^{-1}. Radiation phenomena are negligible in the studied range of temperature.

As the maximal temperature inside the device is located in the silicon chip (the temperature variations at the solder and the heat spreader do not introduce an important thermal conductivity variation in these materials), only the silicon

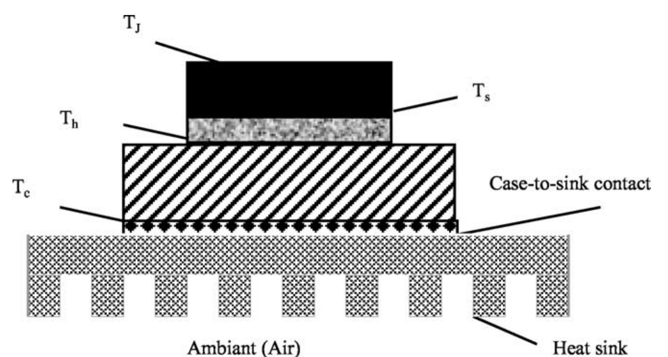

Fig. 7. Multilevel device structure mounted on the heat sink.

Table 1
Thermal characteristics and the identified parameters of the different components constituting the studied devices

Package components	Parameters							
	k (W·m^{-1}·K^{-1})	ρc (J·m^{-3}·K^{-1})	Effective width L (μm)			Effective area S (mm^2)		
			IRGBC 20U	IRGBC 30U	IRGBC 40U	IRGBC 20U	IRGBC 30U	IRGBC 40U
Silicon	134	1.7×10^6	380	460	480	8.4	12.5	20.1
Die bonding	35	1.3×10^6	100	100	100	8.4	12.5	20.1
Heat spreader	143	3.5×10^6	1600	1700	1800	9.8	17.2	29

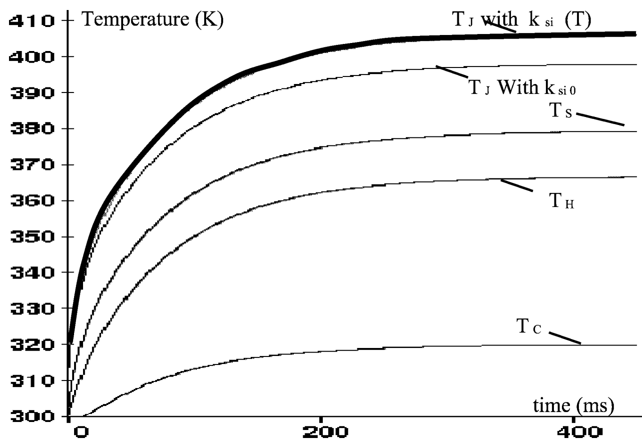

Fig. 8. Temperature responses evolution at different device (IRGBC 20U) level position for a step pumped power (40 W).

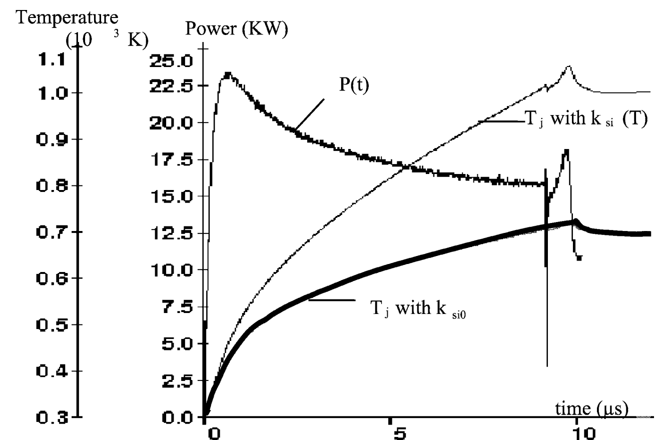

Fig. 9. Junction temperature evolution in the case of a large surge of a short time duration (for the IRGBC 20U).

thermal conductivity non-linearity is taken into account. The thermal resistances between nodes (i and $i+1$) are evaluated with the averaged temperature $T_{i,i+1}$ between these two nodes $T_{i,i+1} = (T_i + T_{i+1})/2$.

The thermal conductivity of silicon is expressed as $k_{\mathrm{Si}}(T) = k_{\mathrm{Si0}}(T/300)^{-4/3}$, where k_{Si0} is the thermal conductivity at room temperature (300 K).

Fig. 8 represents the transient temperature responses at different depths inside the package when the magnitude of the dissipated power step is equal to 40 W. In the case of non-linear thermal conductivity the estimated peak temperature inside the device is larger than the temperature estimated with a constant thermal conductivity. The error is accentuated as the dissipated power increases.

Next section covers the thermal model in the case of large power surges of short time duration.

4. Thermal behavior of the device in the case of large power surges

When the magnitude of the dissipated power is very large (e.g., short circuit conditions), the peak temperature increases rapidly and a high temperature gradient is installed inside the silicon die [9,10]. If no device protection is provided, the device can fail after a short time because of exceeded physical limits of silicon. The junction-to-case thermal impedance curves given by semiconductor manufacturer data-sheets are not valid in the specific case of large power surges of short time duration. However in such a case, the presented model give good results because of the accurate and physical modeling of the silicon chip. Moreover the silicon physical parameters are used, and only equivalent area and length are fitted from transient thermal impedance data.

Fig. 9 shows the peak temperature responses inside the device obtained with a constant (k_{Si0}) and a non-linear thermal conductivity, in the case of short-circuit operating conditions of the IRGBC 20U. The component is short-circuited to 400 V between anode and cathode, and its drive is initially off. A 15 V gate-to-source voltage initiates the short circuit. The dissipated power is obtained experimentally. The estimated peak temperature values are in agreement with the experimental results as detailed in [10]. The device failed after 9 µs of short circuit under 400 V. During this period, the package components (solder and spreader) have no effect on the silicon peak temperature evolution. It means that only the first part (corresponding to duration <10 µs) of the step thermal impedance is required to model the thermal behavior. In the case of large power surges of short time duration a fine mesh in the die is recommended. In the case of the IRGBC 20U, a FEM thermal model of order 12 is sufficient to predict the peak temperature with acceptable accurate with respect to design of power system.

5. Conclusion

A behavioral thermal model of discrete power semiconductor packages is presented. Its main interest is the use of the thermal transient impedance as input data. Such data are obtained by means of experimentation or computed from manufacturer data-sheets. The proposed model is compatible with circuit simulators. An accurate and physical modeling of the semiconductor chip, enables to predict the temperature responses in the case of large power surges of short time duration, that are the practical case in power electronic applications. Moreover, the model takes into account the non-linearities of the silicon thermal conductivity. The identification procedure of the model parameters consists in minimizing the difference between the experimental data and the simulation results based on the relaxation algorithm. The proposed thermal model is easy to implement in any circuit simulator and fruitful for the design of power converter applications.

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